DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5, 31-36, 45, and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 6,253,250 to Evans et al. ("Evans") and US Patent Number 6,996,659 to Lupien et al. ("Lupien").

3. In reference to Claim 1, Evans discloses a method for handling resets at a bus bridge (See Abstract), the method comprising: receiving a reset signal at a bus bridge (See Figure 2 Number 213 and Column 3 Lines 4-6 and 32-37) coupling a master component (See Figure 2 Number 205) supporting a master component bus protocol (See Figure 2 Number 209) to a slave component (See Figure 2 Number 207) supporting a slave component bus protocol (See Figure 2 Number 211), said master component corresponding to a first clock domain (See Figure 2 Number 215) and said slave component corresponding to a second clock domain (See Figure 2 Number 217), wherein the reset signal is associated with a reset of the slave component and not being

associated with the master component (See Column 3 Lines 30-32 and 34-37); synchronizing the reset signal with the first clock domain of the master component such that the master component transitions to an idle state (See Column 5 Line 63 – Column 6 Line 9); resetting said slave component and not resetting said master component (See Column 3 Lines 34-37); and responding to a transaction from the master component to the slave component with a master component bus protocol compliant signal after the reset signal is received (See Figure 5B and Column 5 Line 63 – Column 6 Line 2), wherein the bus protocol compliant signal is a bus signal (See Column 5 Line 63 – Column 6 Line 9), wherein responding with the master component bus protocol compliant signal allows the master component to continue operating without violating said master component bus protocol while the slave component is being reset (See Column 3 Lines 38-51). Evans does not disclose that the first and second domains are different clock domains, and that the bus signal is an Advanced High Performance Bus (AHB) signal. Lupien discloses a bridge device (See Figure 2 Number 100 and Column 1 Lines 5-9) for coupling a master component (See Figure 2 devices coupled to bus 102) corresponding to a first clock domain (See Figure 2 ‘Bus 1 Clock Domain’) to a slave component (See Figure 2 devices coupled to bus 104) corresponding to a second different clock domain (See Figure 2 'Bus 2 Clock Domain'); wherein the bus is an Advanced High Performance Bus (AHB), and thus any signals are AHB signals (See Column 7 Lines 35-39).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the bus bridge of Evans with the bus bridge core for coupling different clock domains of Lupien, resulting in the invention of Claim 1, in order to allow bridging between a wide variety of bus interfaces to be developed quickly (See Column 1 Lines 45-47 of Lupien).

4. In reference to Claim 2, Evans and Lupien disclose the limitations as applied to Claim 1 above. Evans further discloses that the reset signal is received at a bus bridge master interface (See Figure 2 Number 251 and Column 3 Lines 4-6).

5. In reference to Claim 3, Evans and Lupien disclose the limitations as applied to Claim 1 above. Evans further discloses that a bus bridge slave interface (See Figure 2 Number 217) responds with the master component bus protocol compliant signal (See Column 5 Line 63 – Column 6 Line 2).

6. In reference to Claim 5, Evans and Lupien disclose the limitations as applied to Claim 1 above. Lupien further discloses that the master component bus protocol is the AHB protocol operating in a master component clock domain (See Figure 10a).

7. Claims 31-32 recite limitations that are substantially equivalent to those of Claims 1-2 and are rejected under similar reasoning.

8. In reference to Claim 33, Evans and Lupien disclose the limitations as applied to Claim 1 above. Evans further discloses that either the master component or the slave

component is implemented in programmable logic on a programmable device (See Figure 2 Numbers 205 and 207 and Column 3 Lines 14-26). Lupien further discloses that either the master component or the slave component is implemented in programmable logic on a programmable device (See Column 14 Lines 45-54).

9. In reference to Claim 34, Evans and Lupien disclose the limitations as applied to Claim 33 above. Lupien further discloses that either the programmable device is an FPGA (See Column 14 Lines 45-54).

10. In reference to Claim 35, Evans and Lupien disclose the limitations as applied to Claim 1 above. Evans further discloses that responding with a bus protocol compliant signal allows the master component to continue operating without stalling while the slave component is being reset (See Column 3 Lines 38-51 and Column 5 Line 63 – Column 6 Line 9).

11. In reference to Claim 36, Evans and Lupien disclose the limitations as applied to Claim 1 above. Evans further discloses that responding with a bus protocol compliant signal allows the master component to continue operating without locking up while the slave component is being reset (See Column 3 Lines 38-51 and Column 5 Line 63 – Column 6 Line 9).

12. In reference to Claim 45, Evans and Lupien disclose the limitations as applied to Claim 1 above. Evans further discloses that said received reset signal is not associated with a system-wide reset (See Column 2 Lines 35-39 and Column 3 Lines 38-51).

13. Claim 48 recites limitations that are substantially equivalent to those of Claim 45 and is rejected under similar reasoning.

14. Claims 6-8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evans and Lupien as applied to Claim 5 above, and further in view of US Patent Number 6,687,773 to Stewart et al. ("Stewart").

15. In reference to Claim 6, Evans and Lupien disclose the limitations as applied to Claim 5 above. Evans and Lupien do not disclose that the slave component bus protocol is the AHB protocol. Stewart discloses a bridge for coupling an AHB slave component bus protocol (See Figure 1 Number 32 and Column 4 Lines 3-6 and 15-16).

16. It would have been obvious for one of ordinary skill in the art at the time the invention was made to construct the device of Evans and Lupien using AHB as the slave component bus protocol, resulting in the invention of Claim 6, in order to provide a high performance proprietary core integration (See Column 2 Lines 7-32 of Stewart).

17. In reference to Claim 7, Evans and Lupien disclose the limitations as applied to Claim 5 above. Evans discloses that the slave component bus protocol is a PI protocol

(See Figure 2 Number 211 and Column 2 Lines 49-57). Further, the specification discloses the use of either an AMBA bus protocol or a PI bus protocol interchangeably (See Page 11 Paragraph 1), but provides no patentable advantage to either. Thus, the limitation of a PI protocol in the claim is not patentably significant as it relates to the choice of bus protocols selected from a group of equivalents, and thus is not a matter of invention. *In re Yount*, 36 CCPA (Patents) 775, 171 F2.2d 317, 80 USPQ 141.

18. In reference to Claim 8, Evans and Lupien disclose the limitations as applied to Claim 5 above. Evans further discloses synchronizing the reset signal to the master component clock domain (See Figure 2 Number 251).

19. In reference to Claim 10, Evans and Lupien disclose the limitations as applied to Claim 9 above. Evans further discloses setting a bus bridge slave interface (See Figure 2 Number 237) in an idle state while the slave component is being reset (See Column 6 Lines 2-7).

Claim Rejections - 35 USC § 112

20. Claims 1-3, 5-8, 10, 31-36, and 39-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

21. Claims 1 and 31 recite the limitation of “wherein responding…allows the master component to continue operating without violating said master component bus protocol while the slave component is being reset”. The use of the term “allows” does not cause any functionality to occur, as it does not recite what is required, but rather only what is not prohibited. It is thus unclear what Applicant's intended metes and bounds of the claim are, since the claims appear to cover anything and everything that does not prohibit these actions from occurring.

22. Claims 35 and 39 recite the limitation of “wherein responding…allows the master component to continue operating without stalling while the slave component is being reset”. The use of the term “allows” does not cause any functionality to occur, as it does not recite what is required, but rather only what is not prohibited. It is thus unclear what Applicant's intended metes and bounds of the claim are, since the claims appear to cover anything and everything that does not prohibit these actions from occurring.

23. Claims 36 and 40 recite the limitation of “wherein responding…allows the master component to continue operating without locking up while the slave component is being reset”. The use of the term “allows” does not cause any functionality to occur, as it does not recite what is required, but rather only what is not prohibited. It is thus unclear what Applicant's intended metes and bounds of the claim are, since the claims appear to cover anything and everything that does not prohibit these actions from occurring.

24. Dependent claims inherit the indefiniteness of their parent claims and are rejected under the same reasoning.

Allowable Subject Matter

25. Claims 11, 13-20, 24-30, 37-38, 41-44, and 46-47 are allowed.

26. Claims 39-40 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

27. The following is an examiner's statement of reasons for allowance and indication of allowable subject matter: The claims are allowable for the reasons previously indicated. For the purpose of evaluating prior art with respect to patentability, the Examiner has interpreted the "alternating state handler" in accordance with Applicant's description in Paragraphs 1-2 of Page 13 and In Figure 4.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Drawings

28. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Figure 1 is identified in the specification as “a typical computer system” (See Page 9 Lines 6-8 and Page 10 Lines 1-2). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Oath/Declaration

29. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

30. The oath or declaration is defective because: Non-initialed and/or non-dated alterations have been made to the oath or declaration. See 37 CFR 1.52(c). Alterations to the address of inventor Andrew Crosland have been made

Response to Arguments

31. Applicant's arguments filed 2 February 2009 have been fully considered but they are not persuasive.

32. Applicant has argued that neither Evans nor Lupien disclose that responding with the bus protocol compliant signal allows the master to continue operating without violating bus protocols while the slave component is being reset (See Page 11 Paragraph 4 - Page 12 Paragraph 1). In response, the Examiner notes that Evans discloses that the reset on the second bus is isolated and not propagated to the first bus, thus preventing interruption during operation of devices on the first bus (See Column 3 Lines 39-51). Further, as indicated above, The use of the term “allows” does not cause any functionality to occur, as it does not recite what is required, but rather only what is not prohibited. The combination of Evans and Lupien does not prohibit the master from continuing to operate without violating bus protocols while the slave component is being reset.

33. Applicant has argued that limitations from Claim 4 (previously indicated as allowable) have been incorporated into Claims 1 and 31 (See Page 12 Paragraph 2). In response, the Examiner notes that not all of the limitations of Claim 4 as previously presented have been incorporated into Claims 1 and 31.

Conclusion

34. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: “Advanced Microprocessor Bus Architecture (AMBA) Bus System” by Ray Weiss, which discloses that the use of an AHB bus is notoriously old and well known in the art; US Patent Number 6,108,778 to LaBerge, which discloses blocking bus transactions during a reset; and US Patent Application Publication Number 2002/0015565 to Imamura, which discloses a bridge which blocks resets from propagating through an entire network.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Cleary whose telephone number is (571)272-3624. The examiner can normally be reached on Monday-Thursday (7-3).

If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Mark Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thomas J. Cleary/
Patent Examiner, Art Unit 2111